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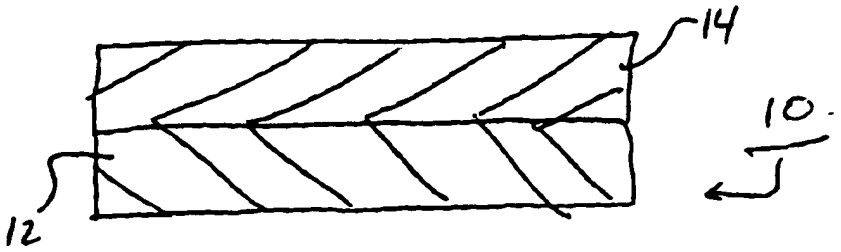
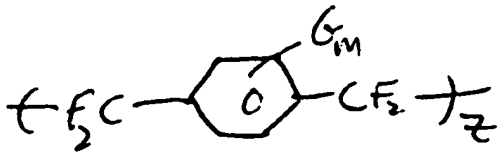
(54) Title: PARYLENE POLYMER LAYERS

(57) Abstract

Multi-level structures including a first layer with a parylene polymer layer deposited thereon. The parylene polymer layer has structure (I), wherein m is an integer having a value of 0, 1, 2, 3 or 4, and z is greater than 1. G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$. X is a halogen, and n is an integer greater than zero. The sum of y and w is at most equal to a 2n+1. The parylene polymer layer has a zinc impurity level of at most about 10 parts per million. In certain embodiments, the parylene polymer layer may have a zinc impurity level of less than 50 parts per billion. The parylene polymer layers are formed by a process in which monomers are formed outside of a deposition zone of a vacuum chamber. The monomers may be prepared by a process in which a parylene dimer is vaporized and subsequently pyrolized. The process may further include the step of passing the vapor through a post-pyrolysis zone prior to depositing the monomer on the substrate.





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PARYLENE POLYMER LAYERS

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates generally to parylene polymer layers, and more specifically to such layers which are disposed between electrically conductive layers in integrated circuits.

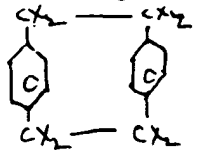
2. Discussion Of The Related Art

Semiconductors are widely used in integrated circuits for electronic products systems such as computers and televisions. These integrated circuits typically combine many transistors on a single crystal silicon chip to perform complex functions and store data. Semiconductor and electronics manufacturers, as well as end users, desire integrated circuits which can accomplish more in less time in a smaller package while consuming less power. However, some of these desires may be in opposition to each other. For example, simply shrinking the feature sizes on a given circuit from 0.5 microns to 0.25 microns can increase power consumption by 30%. Likewise, doubling operational speed generally doubles power consumption. Miniaturization also generally results in increased capacitive coupling, or cross talk, between conductors which carry signals across the chip. This can limit achievable speed and degrade the noise margin used to insure proper device operation.

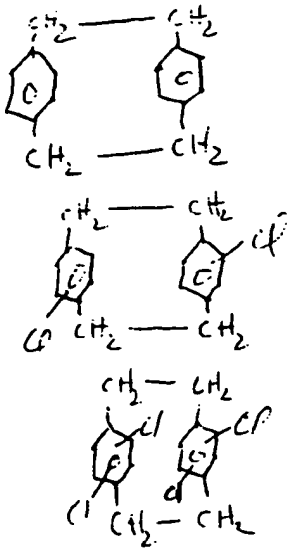
One way to diminish power consumption and cross talk effects is to decrease the dielectric constant of electrically insulating layers that separate layers of electrically conductive materials within the integrated circuit. In addition, since operational conditions may include high temperatures, it can be advantageous to use materials with relatively high thermal stability to form the insulating layers.

Silicon dioxide is one of the most common materials used in insulating layers for integrated circuits. However, silicon dioxide is non-ideal due to its comparatively high dielectric constant of about 3.9.

Layers formed from parylene polymers have been proposed for use as insulating layers in integrated circuits because these materials have relatively low dielectric constants and comparatively high melting temperatures. Parylene polymers are poly-p-xylylenes which may be prepared starting with a dimer having the structure:

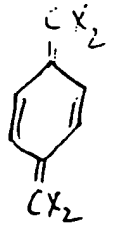


wherein X is typically a hydrogen or a halogen. The most common forms of parylene dimers include the following:



Polymer films formed from these parylene dimers may have comparatively low dielectric constants and relatively high melting temperatures. However, these parylene polymer films have relatively high dielectric constants and inferior thermal stabilities, rendering them less attractive for use in integrated circuits.

Typically, a vapor deposition method is used to form parylene polymer layers from parylene dimers. One such vapor deposition method is disclosed in *Journal of Applied Polymer Science* 13, 2325 (1969). According to this method, commonly referred to as the Gorham process, the parylene dimer is cracked at an elevated temperature to produce parylene monomer having the structure:



The parylene monomer is condensed onto a substrate at a temperature of from about room temperature to about -35°C. Under these conditions, the parylene monomer simultaneously polymerizes on the substrate to form a layer of the parylene polymer adhered to the substrate.

A vapor deposition process for forming poly-p-xylylene films from other than parylene dimer materials is disclosed in U.S. Patent No. 5,268,202 (You). The method disclosed by this reference includes forming the monomer vapor inside the vacuum chamber in which deposition occurs, precluding the purification opportunities afforded by the parylene dimer process prior to deposition on the substrate. Therefore, the resulting poly-p-xylylene layers have relatively high impurity levels. For example, *Journal of Vacuum Science and Technology* A11(6), 3057 (1993) discloses that poly-p-xylylene films formed by the method of You have zinc impurity levels of about 3%. Such a comparatively high level of zinc impurity results in problems with the poly-p-xylylene film relating to, for example, increased dielectric constant, decreased surface resistivity, ion movement within the layer, film surface charging effects and/or electron storm formation when the poly-p-xylylene film is used within a multi-level structure. As a result, these poly-p-xylylene films cannot be used in integrated circuits.

Hence, it remains a challenge in the art to provide an electrically insulating layer for use in integrated circuits of electronic devices that has a relatively low dielectric constant and comparatively high melting temperature. It is a further challenge in the art to provide such an insulating layer which is formed from a parylene polymer.

SUMMARY OF THE INVENTION

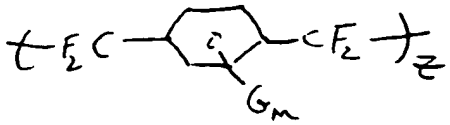
Therefore, it is an object of the present invention to provide parylene polymer layers having relatively low dielectric constants and comparatively high melting temperatures.

It is another object of the present invention to provide methods of making such parylene polymer layers.

It is another object of the present invention to provide multi-level structures that include such parylene polymer layers.

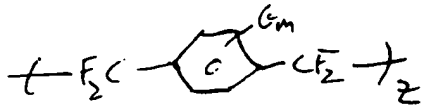
It is a further object of the present invention to provide methods of making such multi-level structures.

In one illustrative embodiment, the present invention provides a multi-level structure that includes a first layer and a parylene polymer layer disposed along the first layer. The parylene polymer layer is formed from a material having the structure:



m is an integer having a value of 0, 1, 2, 3 or 4, and z is greater than 1. G is a halogen, alkyl group, cyclo hydrocarbon, alkylene group or alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero. If G is an alkyl group, y +w equals 2n+1, but if G is a cyclo hydrocarbon, alkylene group or an alkylyne group, y + w is less than 2n+1. The parylene polymer layer has a zinc impurity level of at most about 10 parts per million.

In another illustrative embodiment, the present invention provides a method making a multi-level structure. The method includes the steps of depositing a monomer on a surface of a first layer and polymerizing the monomer to form a parylene polymer film on the surface of the first layer. The parylene polymer has the structure:



m is an integer having a value of 0, 1, 2, 3 or 4, and z is greater than 1. G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero. If G is an alkyl group, y +w equals 2n+1, but if G is a cyclo hydrocarbon, alkylene group or an alkylyne group, y + w is less than 2n+1. The parylene polymer layer has a zinc impurity level of at most about 10 parts per million.

In a further illustrative embodiment, the present invention provides a multi-level structure that comprises a first layer and a parylene polymer layer disposed along the surface of the first layer. The parylene polymer layer is formed from a material having the structure:

m is an integer having a value of 0, 1, 2, 3 or 4, and z is greater than 1. G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero. If G is an alkyl group, y +w equals 2n+1, but if G is a cyclo hydrocarbon, alkylene group or an alkylyne group, y + w is less than 2n+1. The parylene polymer layer has a zinc impurity level of at most about 10 parts per million. The multi-level structure is formed by a process that includes: vaporizing a parylene dimer; and pyrolizing the parylene dimer to form a monomer.

In one aspect, it is a feature of the present invention to provide parylene polymer films that can be effectively used in relatively harsh environments, such as, for example, high temperature (e.g., above about 200°C), high corrosion or both.

BRIEF DESCRIPTION OF THE DRAWINGS

The advantages and features of the present invention will be more clearly understood in view of the following detailed description when taken in conjunction with the drawings, in which:

Fig. 1 is a cross-sectional view of one embodiment of a multi-level structure according to the present invention;

Fig. 2 is a cross-sectional view of another embodiment of a multi-level structure according to the present invention;

Fig. 3 is a cross-sectional view of a portion of one embodiment of an integrated circuit including a multi-level structure according to the present invention; and

Fig. 4 is a block diagram of one embodiment of a vacuum chamber which may be used to form parylene polymer layers according to the present invention.

DETAILED DESCRIPTION

Fig. 1 depicts a multi-level structure 10 according to the present invention. Structure 10 includes substrate layer 12 and parylene polymer layer 14. By "parylene polymer" it is herein meant to refer to a poly-p-xylylene formed from a parylene dimer.

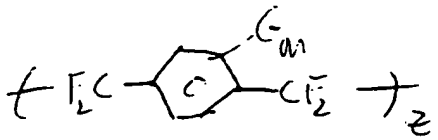
Substrate layer 12 may be formed from any materials onto which parylene polymer layer 14 is capable of being deposited. These materials may include electrically conductive and electrically non-conductive materials. The particular material from which layer 12 is formed

depends upon the application, and such materials are known to those skilled in the art. For example, substrate layer 12 may be formed from organic materials or inorganic materials including, but not limited to, aluminum, iron, steel, molybdenum, aluminum oxide, titanium oxide, lead oxide, copper oxide, iron oxide, beryllium oxide, manganese oxide, tungsten oxide, tantalum oxide, vanadium oxide, silicones, natural rubbers, plastics, plastic composites, cellulosic materials, epoxy-containing compounds, thermosetting compounds, thermoplastic compounds, oxides of silicon (e.g., fly ash, hydrated silica, silica, quartz, aerogels, xerogels and fumed silica) and the like. Furthermore, layer 12 may comprise gallium arsenide or other binary semiconductors.

Substrate layer 12 may also be formed from a vacuum compatible liquid. By "vacuum compatible" it is herein meant to refer to a material that has a vapor pressure at the operating temperature of the vacuum chamber used such that the minimum pressure to which the vacuum chamber can be pumped is independent of the presence of the vacuum compatible material. One example of a vacuum compatible liquid is gamma-methacryloxypropyltrimethoxysilane.

In certain embodiments, substrate layer 12 may be a printed circuit board, a silicon backboard, a fiberglass backboard, a silicon wafer, paper, a key pad, a catheter, a pacemaker cover, a subcutaneous probe, a bird feather, a silicone O-ring, parts of a mechanical apparatus, such as an automobile, or the like.

Parylene polymer layer 14 is formed from a material having the structure:



m is an integer having a value of 0, 1, 2, 3 or 4, and z is greater than 1. G is a halogen, an alkyl group, a cyclo hydrocarbon an, alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero and z is 1. If G is an alkyl group (i.e., saturated) then y +w = 2n+1. If G is a cyclo hydrocarbon, an alkylene or alkylyne group (i.e., G has at least one degree of unsaturation) then y + w is less than 2n+1 by a factor of twice the degree of unsaturation.

Fig. 2 depicts another multi-level structure 20 according to the present invention. Structure 20 includes parylene polymer layer 14 disposed between a first layer of material 16 and a second layer of material 18. Although not limited to these materials, layers 16 and 18 may be formed from any of the materials listed above with reference to substrate layer 12. Furthermore, layer 16 and/or layer 18 may take on any of the above-noted shapes of substrate layer 12. Layer 16 and/or layer 18 may take on other shapes as well.

In certain embodiments, each of layers 16 and 18 may be formed from materials that are at least partially electrically conductive. In such embodiments, layers 16 and 18 may be formed from metals using standard photolithographic and etching techniques. For these embodiments, layers 16 and 18 may each correspond to a power plane, a ground plane or a metal interconnection trace layer. Other processes for forming layers 16 and 18 are known to those skilled in the art and are intended to be within the scope of the present invention.

Parylene polymer layer 14 may be relatively difficult to adhere to certain other materials, so it may be desirable to promote the adhesion of layer 14 to other surfaces. Accordingly, parylene polymer layer 14 may undergo certain surface treatments to increase its ability to adhere to other surfaces. Such treatments include, for example, plasma treatment, corona treatment, charge treatment and/or other surface roughening treatments. These treatments are known to those skilled in the art and are intended to be within the scope of the present invention. These surface treatments may be performed on the entire surface of layer 14 or only on portions thereof. Furthermore, in some embodiments, layer 16 and/or layer 18 may be formed from a material that promotes adhesion between parylene polymer layer 14 and other layers. For such embodiments, layer 14 may or may not undergo any of the above-noted surface treatments.

For some applications, it may be advantageous to prevent the diffusion of materials through parylene polymer layer 14. For these applications, layer 16 and/or layer 18 may be formed from materials that reduce or eliminate the diffusion of materials through parylene polymer layer 14. Materials appropriate for use in these applications are disclosed in, for example, U.S. Patent No. 5,470,802. Other such materials are known to those skilled in the art and are intended to be within the scope of the present invention.

For certain uses, such as, for example, electronic circuits, it may be desirable to form relatively flat layers, but, since parylene polymer layer 14 is comparatively conformal, layer 14 may not have the desired degree of flatness. Hence, it may be advantageous to grind or otherwise treat layer 14 to make it more flat, often referred as planarizing within the art.

However, in certain embodiments, layer 14 may be difficult to planarize. For these embodiments, layer 16 and/or layer 18 may be formed from a material that is more readily planarized. Typically, such a material is a dielectric material, but, in some instances, it may be an electrical conductor.

Fig. 3 shows a portion 30 of a multi-level electronic circuit according to the present invention. Portion 30 includes silicon wafer substrate 22, electrically insulating layer 24, electrically conductive layer 26, electrically conductive layer 28 and parylene polymer layer 14 disposed between layers 26 and 28.

Silicon wafer substrate 22 may be formed from any of the standard substrate materials used in the electronics industry, such as, for example, a silicon backboard or a fiberglass backboard. Other appropriate structures for wafer substrate 22 are known to those skilled in the art and are intended to be within the scope of the present invention.

Electrically insulating layer 24 typically functions to protect wafer substrate 22 from electrically conductive layers 26 and 28. Layer 24 is usually formed from silicon dioxide, although other appropriate materials may be used. Electrically insulating layer 24 may be formed according to any of the standard techniques known to those skilled in the art.

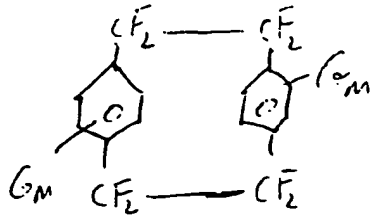
Electrically conductive layers 26 and 28 may be formed from metals or other materials appropriate for use in electronic circuits. Layers 26 and 28 may comprise metal conductor lines which are formed according to standard photolithographic and etching techniques. For such embodiments, layers 26 and 28 may each correspond to a power plane. a ground plane or an interconnection trace layer.

Electrically conductive layers 26 and 28 may be interconnected through parylene polymer layer 14 by use of vias, or through holes (not shown), which are formed in parylene polymer layer 14 by conventional processees known to those skilled in the art.

According to the present invention, parylene polymer layer 14 is formed using a vapor deposition process. Preferably, the vapor deposition process allows the monomer to be formed outside the deposition portion of the vacuum chamber such that the monomers can undergo a purification process prior to being deposited onto the substrate. In a particularly preferred embodiment, parylene polymer layer 14 is formed using a vacuum chamber 40 as depicted in Fig. 4. Vacuum chamber 40 includes vaporization zone 42, a pyrolysis zone 44, a post-pyrolysis zone 46 and a deposition zone 48. Examples of such vacuum chamber are disclosed in, for

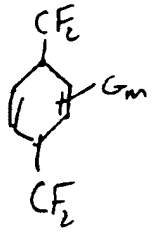
example, commonly assigned U.S. Patent No. 5,546,473, which is herein incorporated by reference.

A dimer material having the structure:



is placed within vaporization zone 42 at about room temperature and subsequently heated to a temperature of from about 70°C to about 150°C to vaporize the dimer.

The vaporized dimer passes into pyrolysis zone 44 which is maintained at a temperature of from about 600°C to about 720°C to pyrolize the dimer (i.e., cleave certain chemical bonds) and form a monomer having the following structure:



The monomer passes through post-pyrolysis zone 46 which is maintained at a temperature of at most about room temperature. At this temperature, residual vaporized dimer can adhere to the walls of post-pyrolysis zone 46 while the monomer generally passes through post-pyrolysis zone 46 without adhering to the walls of zone 46. Thus, post-pyrolysis zone 46 reduces the amount of vaporized dimer that ultimately enter deposition chamber 48. In certain embodiments, this feature can be advantageous because the vaporized dimer can constitute an impurity in parylene polymer layer 14, which may have an undesirable local effect on the dielectric constant or other properties of layer 14.

After passing through post-pyrolysis zone 46, the monomer enters deposition chamber 48 which includes substrate 50. Substrate 50 is placed on a platen 52 that includes a standard temperature controlling device 54 that controls the temperature by the platen by heating and/or

cooling platen 54. By use of device 54, the temperature of substrate 50 and platen 52 is typically held at a temperature of from about room temperature to about -25°C during deposition of the monomer onto substrate 50.

It has been found that reducing the temperature of substrate 50 and platen 52 during monomer deposition can provide several advantages, including more control of the overall process of making parylene polymer layer 14 by allowing for increased manipulation of the monomer. For example, cooling substrate 50 and platen 52 allows for the walls of deposition chamber 48 to be heated during monomer deposition. In addition, reducing the temperature of substrate 50 and platen 52 during monomer deposition results in a more efficient deposition process and a more efficient use of the parylene dimer starting material.

Subsequent to monomer deposition, device 54 may be used to increase the temperature of substrate 50 and platen 52 to a temperature of from about 100°C to about 400°C to anneal the parylene polymer layer. However, it is to be noted that polymerization of the parylene monomer occurs spontaneously at the temperatures of substrate 50 noted above.

Prior to placing the dimer within vaporization zone 46, the dimer is first purified. Since the dimer of the present invention has a high degree of symmetry, it is readily purified by crystallization. Typically, these solvents are relatively unsymmetric in order to have a high temperature coefficient of solubility. However, if the solvent is too symmetric, separation of the solvent from the dimer may be difficult. Without wishing to be bound by any theories, it is believed that this increased difficulty in solvent/dimer separation results from the accidental accommodation of the solvent within the dimer lattice. Solvents appropriate for use in dimer crystallization according to the present invention include, but are not limited to, chloroform, tetrahydrofuran, methylene chloride, and linear hydrocarbons such as n-hexane and n-heptane. In a preferred embodiment, the solvent is n-hexane.

Using this process has been found to produce parylene polymer layers which have reduced levels of impurities. For example, parylene polymer layers in accordance with the present invention may have zinc impurity levels of 10 parts per million or less. In some embodiments, the zinc impurity level may be less than 50 parts per billion. This feature of the present invention is desirable because impurities within parylene polymers can result in several different negative effects, including, but not limited to, an increase in the dielectric constant of the parylene polymer layer, a decrease in the surface resistivity of the parylene polymer layer and/or electron storm formation within the multi-level structure.

While particular apparatuses and methods of making parylene polymer layer 14 have been described herein, one skilled in the art would understand that at least certain aspects of these apparatuses and methods may be varied or modified, and such variations and modifications are intended to be within the scope of the present invention. For example, in addition to cleaving the parylene dimer bond by use of elevated temperature as discussed above, the parylene dimer may be cleaved by use of a plasma. Such methods are disclosed in, for example, Russian Patent Nos. RU 2,000,850 and RU 2,002,519.

When used in integrated circuits or for other electronics applications, parylene polymer layer 14 should have a minimal dielectric constant to enhance circuit operating speed and decrease power consumption. Accordingly, these parylene polymer layers preferably have a dielectric constant of at most about 2.6, more preferably at most about 2.4 and most preferably at most about 2.2.

Having a low dissipation factor decreases the signal loss in an integrated circuit. Therefore, parylene polymer layers in accordance with the present invention preferably have a dissipation factor of less than about 0.001.

According to the present invention, parylene polymer layers with a thickness of about one micrometer preferably have a breakdown voltage of at most about 750 microvolts.

Parylene polymer layer 14 preferably has a Young's modulus of about 5 gigapascals.

The elongation to break of parylene polymer layers according to the present invention is preferably at least about 20%.

Parylene polymer layer 14 preferably has an ultimate tensile strength of at least about 122 megapascals.

According to the present invention, parylene polymer layers have water absorption values of at most about 0.5% by weight, more preferably at most about 0.2% by weight and most preferably at most about 0.1% by weight.

Parylene polymer layers in accordance with the present invention preferably have a thermal stability such that these layers demonstrate less than 1% weight loss per 2 hours at a temperature of at least about 450°C.

Parylene polymer layer 14 preferably has a crystalline melting point of above about 500°C.

The surface resistivity of parylene polymer layers in accordance with the present invention is preferably about 1.3×10^{14} ohms.

The volume resistivity of parylene polymer layer 14 is preferably about $5.3x10^{16}$ ohms.

Parylene polymer layers in accordance with the present invention preferably have a density of about 1.58.

The thermal expansion at 25°C of parylene polymer layer 14 is preferably at most about 35 parts per million.

According to the present invention, parylene polymer layers have a coefficient of friction of about 0.2.

The following is an illustrative example of one embodiment of the present invention. It is not to be construed as limiting.

Example

The following process was performed in a jacketed Soxhlet extractor (available as catalog number LG-6950, from Lab Glass, located in Vineland, NJ or as catalog number CG-1328, available from Chem Glass, located in Vineland, NJ). An amount of the crude dimer used as the starting material in the synthesis of the parylene polymer layers of the present invention was placed within a glass extraction thimble with a fritted glass disk at its bottom. A short chromatographic bed of particulate alumina was placed at the bottom of the thimble. The thimble was purchased with a diameter of 41 mm and a height of 130 mm. The height of the thimble was increased to 180 mm to accommodate larger samples (i.e., up to about 70 grams) of the crude dimer.

A flask of boiling n-hexane was placed below the thimble, and gaseous n-hexane was condensed in a condenser mounted above the thimble. The condensed n-hexane dripped onto the crude dimer to form a leachant solution of the condensed n-hexane, purified dimer and impurities, including dirt, dust, and/or polymers or oligomers of the monomer formed by the dimer. The leachant solution passed through the chromatographic bed and fritted glass at the bottom of the thimble. The chromatographic bed removed many polar or ionic impurities present within the leachant solution due to the polar nature of alumina. In addition, the chromatographic bed removed fine impurities by filtration.

A siphoning mechanism was used to periodically empty the leachant solution from the Soxhlet extractor holding the thimble. This process returned the n-hexane from the leachant solution to the flask of boiling n-hexane. After a period of from about 10 to about 20 hours, the crude dimer ended up in the flask of boiling n-hexane.

The extraction was conducted at the boiling n-hexane to speed up the dimer dissolution process. To accomplish this, a conduit jacket surrounded the extraction volume, so the extraction volume was heated by vapors of n-hexane as these vapors traveled from the boiling flask to the condenser. While this hot filtration process is advantageous because impurities are removed while the solution is hot, it is to be noted that, in conventional crystallization equipment, such a hot filtration can be difficult and/or dangerous when flammable solvents are used. Furthermore, for practical reasons, such a filtration may be performed at temperatures below the solvent boiling temperature, resulting in increased solvent use and decreased dimer solubility. However, using a Soxhlet apparatus, the boiling solvent vapors are held within the apparatus by the jacket, allowing for increased efficiency in the purification process.

The resulting purified dimer of the present invention was tested by inductively coupled plasma-mass spectrometry of the vaporized dimer. During this process, the sample is ashed to remove carbon containing components, leaving nonvolatile oxides of the trace elements to be determined. This ash is taken up in an aqueous buffer solution. The aqueous buffer solution of the sample ash is fed to an energized plasma. The high temperature of the plasma atomizes the trace elements. The atomized plasma is fed to the source of a mass spectrometer for quantification of each specific impurity elements.

The results are shown in Table 1, which clearly demonstrates that the zinc impurity levels are less than about 50 parts per billion. This method does not involve a direct measurement of the impurity level of the parylene polymer layer formed from the monomers. However, by measuring the impurity level of the starting material (i.e., dimer) for parylene polymer film synthesis, this method does provide an upper limit on the possible impurity level of the parylene polymer films of the present invention.

Table 1

Element	Impurity Level (Parts per Billion)
Al	<100
Ba	<10
Be	<10
Bi	<10
Cd	<10

Element	Impurity Level (Parts per Billion)
Ca	<100
Cs	<250
Cr	<10
Co	<1
Cu	<10
Ga	<1
In	<10
Fe	<100
Pb	<10
Li	<200
Mg	<100
Mn	<10
Mo	<1
Ni	<10
K	<50
Rb	<1
Ag	<1
Na	<400
Sr	<10
Th	<1
Sn	<700
V	<1
Zn	<50
Zr	<1

To purify about 70 grams of crude dimer according to this process, about 3 liters of n-hexane may be used. In this embodiment of the process, a 1 liter flask having an initial volume of about 0.7 l of n-hexane is utilized.

Having thus described particular embodiments of the present invention, various alterations, modifications and improvements will readily occur to those skilled in the art. Such alterations, modifications and improvements are intended to be part of this disclosure, and are intended to be within the spirit and scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended as limited. The present invention is limited only as defined by the following claims and the equivalents thereto.

CLAIMS

1. A multi-level structure, comprising:

a first layer having a surface; and

a parylene polymer layer disposed along the surface of the first layer, the parylene polymer layer being formed from a material having a structure:

wherein m is an integer having a value of 0, 1, 2, 3 or 4, z is greater than 1, G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero and a sum of y and w is at most equal to a sum of 2n and 1, and wherein the parylene polymer layer has a zinc impurity level of at most about 10 parts per million.

2. The multi-level structure according to claim 1, further comprising a second layer having a surface, wherein the parylene polymer layer is disposed along the surface of the second layer such that the parylene polymer layer is disposed between the first and second layers.

3. The multi-level structure according to claim 2, wherein the first layer is an electrically conductive material.

4. The multi-level structure according to claim 3, wherein the second layer is formed from an electrically conductive material.

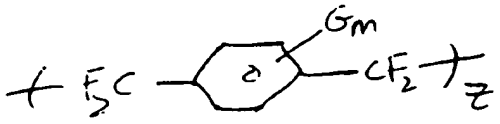
5. The multi-level structure according to claim 1, wherein the parylene polymer layer has a dielectric constant of at most about 2.6.

6. The multi-level structure according to claim 1, wherein the parylene polymer layer has a zinc impurity level of at most about 50 parts per billion.

7. A method making a multi-level structure, comprising the steps of:

depositing a monomer on a surface of a first layer; and

polymerizing the monomer to form a parylene polymer film on the surface of the first layer, the parylene polymer having a structure:



wherein m is an integer having a value of 0, 1, 2, 3 or 4, z is greater than 1, G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero and a sum of y and w is at most equal to a sum of 2n and 1, and wherein the parylene polymer layer has a zinc impurity level of at most about 10 parts per million.

8. The method according to claim 7, further comprising the steps of:

vaporizing a parylene dimer; and

pyrolizing the parylene dimer to form the monomer.

9. The method according to claim 8, wherein the depositing step occurs in a deposition zone of a vacuum chamber.

10. The method according to claim 9, wherein the pyrolizing step occurs outside the deposition zone of the vacuum chamber.

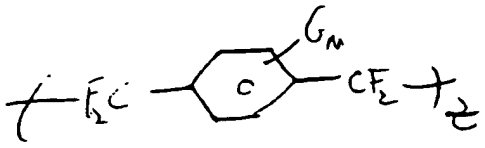
11. The method according to claim 10, further comprising the step of feeding the monomer into the deposition zone of the vacuum chamber.

12. The method according to claim 10, wherein the polymerizing step includes polymerizing the monomer to form a parylene polymer film having a zinc impurity level of at most about 50 parts per billion.

13. A multi-level structure, comprising:

a first layer having a surface; and

a parylene polymer layer disposed along the surface of the first layer, the parylene polymer layer being formed from a material having a structure:



wherein m is an integer having a value of 0, 1, 2, 3 or 4, z is greater than 1, G is a halogen, an alkyl group, a cyclo hydrocarbon, an alkylene group or an alkylyne group having the general formula $C_nH_yX_w$, wherein X is a halogen, n is an integer greater than zero, and a sum of y and w is at most equal to a sum of 2n and 1, and wherein the parylene polymer layer is formed by a process including the steps of:

vaporizing a parylene dimer; and

pyrolizing the parylene dimer to form a monomer.

14. The multi-level structure according to claim 13, wherein the process further comprises the step of depositing the monomer on a surface of a first layer.

15. The multi-level structure according to claim 14, wherein the depositing step occurs within a deposition zone of a vacuum chamber.

16. The multi-level structure according to claim 15, wherein the pyrolizing step occurs outside the deposition zone of the vacuum chamber.

17. The multi-level structure according to claim 16, wherein the process further includes the step of polymerizing the monomer on the surface of the first layer to form the parylene polymer layer.

18. The multi-level structure according to claim 17, wherein the process includes the step of feeding the monomer into a deposition zone of a vacuum chamber.

19. The multi-level structure according to claim 18, wherein the multi-level structure has a zinc impurity level of at most about 10 parts per million.

20. The multi-level structure according to claim 13, wherein the parylene polymer layer has a zinc impurity level of at most about 10 parts per million.

21. The multi-level structure according to claim 20, wherein the parylene polymer layer has a dielectric constant of at most about 2.6.

22. The multi-level structure according to claim 13, wherein the parylene polymer layer has a dielectric constant of at most about 2.6.

23. The multi-level structure according to claim 13, wherein the parylene polymer layer has a zinc impurity level of at most about 50 parts per billion.

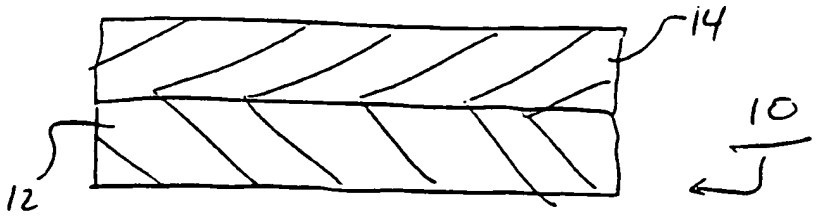


FIG. 1

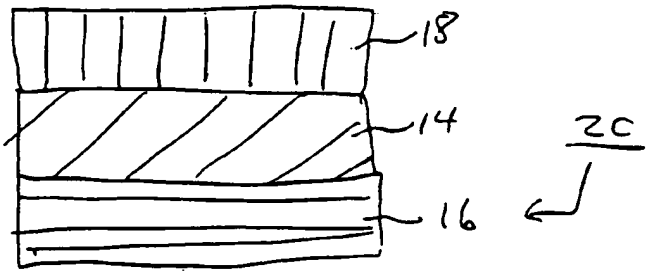


FIG. 2

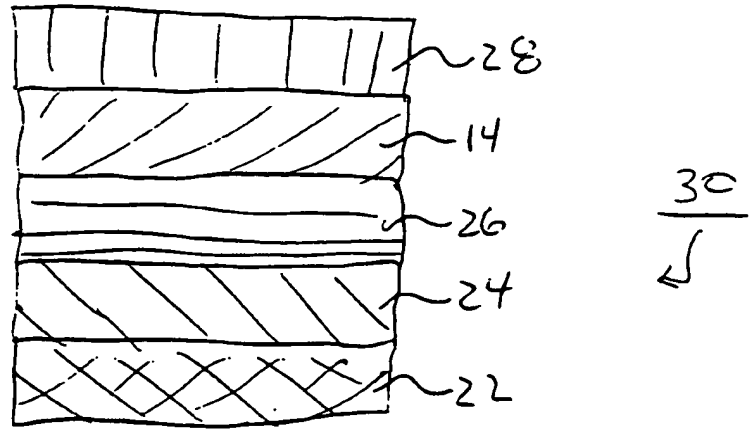


FIG. 3

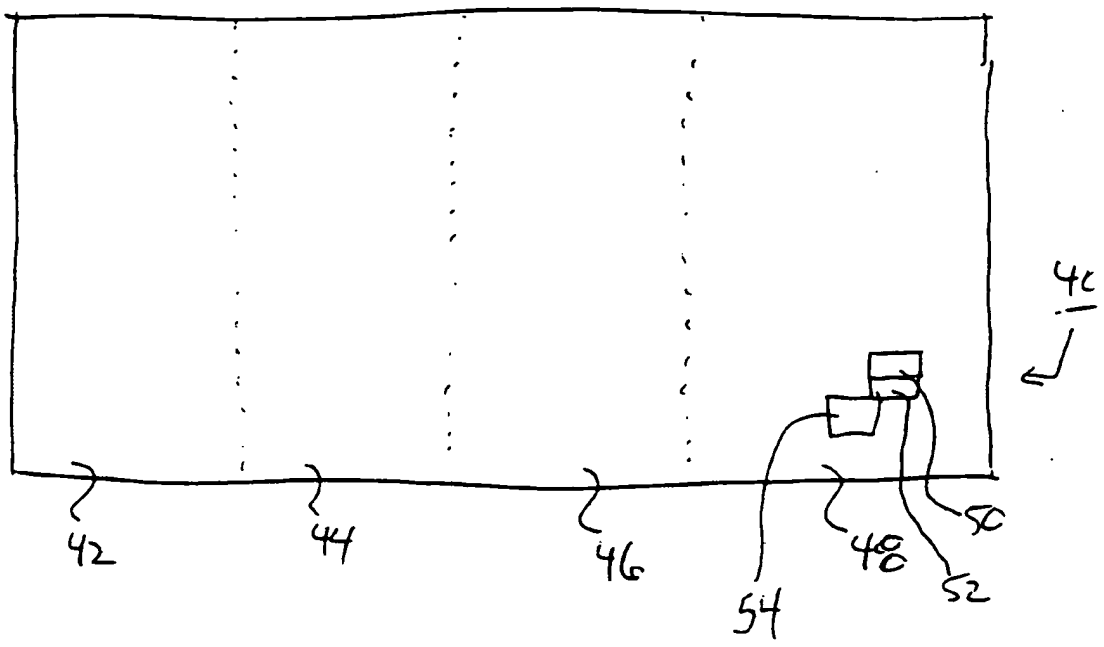


FIG. 4

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 96/17052

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/522 C08G61/02 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 C09D H01L C08G C08L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,3 332 891 (SUI-WU CHOW) 25 July 1967 see claims; examples ---	1-23
X	US,A,3 274 267 (SUI-WU CHOW) 20 September 1966 see claims; examples ---	1-23
A	GB,A,1 146 005 (UCC) 19 March 1969 see page 4, line 76 - page 6, line 113; claims ---	1
A	US,A,3 319 141 (F.E. CARLTON, E.A.) 9 May 1967 see claims ---	1
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search	Date of mailing of the international search report
20 December 1996	09.01.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Deraedt, G

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INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/US 96/17052

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CHEMICAL ABSTRACTS, vol. 121, no. 18, 31 October 1994 Columbus, Ohio, US; abstract no. 207149, DABRAL, S, E.A.: "Fluorinated parylene as an interlayerdielectric for thin film MCM's" XP002021764 see abstract & MATER. RES. SOC. SYMP. PROC., 1992, pages 83-89,	1
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A	CHEMICAL ABSTRACTS, vol. 82, no. 16, 21 April 1975 Columbus, Ohio, US; abstract no. 98821, BABIZHAEV, V M , E.A.: "Poly(alpha.,alpha.,alpha',alpha'-tetrafluoro-p-xylylene)" XP002021765 see abstract & SU,A,443 891	1

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INTERNATIONAL SEARCH REPORT

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PCT/US 96/17052

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		GB-A-	1086714	
		NL-A-	6411018	24-03-65
		NL-A-	6411020	24-03-65
		NL-A-	6411094	24-03-65
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		NL-A-	6411019	24-03-65
		GB-A-	1074708	
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		NL-A-	6411018	24-03-65
		NL-A-	6411020	24-03-65
		NL-A-	6411094	24-03-65
		US-A-	3332891	25-07-67
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US-A-3319141	09-05-67	NONE		